6	2	9	1	July 83

PB0-PB7, CB1, CB2

PRINTER CONNECTOR
BUSY
ACKNOWLEDGE
DATA 6 (MSB)
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA 0 (LSB)
STROBE
PL2
0V
IC8 74LS244
IC7 6522A
R2 4K7
R3 4K7
+5V

IC5 MC68B50
DCD
RTS
CTS
TxD
RxD
TxC
RxC

IC6 MC14411
XI
XO
XL1
1.8432 MHz
R1 15M
LK9

PARALLEL INTERFACE CONNECTOR
PL4
IC4 INS 8255
IC4 NOT FITTED FOR SYSTEM 5

IC9 74LS04
LK4
INTERRUPT SELECT

SIDE B
SIDE A

REQUEST TO SEND
CLEAR TO SEND
COMMON
DATA OUTPUT
DATA INPUT
TTY OUT +VE
TTY OUT -VE
TTY IN +VE
TTY IN -VE
PINS 5-12 ARE TO RS232C (V24) SPEC
PINS 1-4 ARE FOR A 20mA LOOP
PL3
LK8
Q1 BC309
Q2 BC239
Q3 BC 239
Q4 BC309
Q5 BC239
Q6 BC 239
Q7 BC239
D1 1N4148
D2 1N4148
D3 1N4148
IC10 TIL112
+12V
-12V

LK1
LK2

AD1D 12A10
+5V, VCC, VDD
0V, GND, VSS
C1 22µ 16v
C2 47nF
C3 47nF
C4 47nF
C5 47nF
C6 47nF
C7 47nF
C8 47nF

LK6
IC3 74LS139
HALF PAGE SELECT
CHIP SELECT

LK7
IC2 74LS138
PAIR OF PAGES DECODE

LK5
IC1 74LS138
BLOCK DECODE (OPTIONAL)

PRELIMINARY ISSUE
DATE 27 JUN 1983

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DATE 6 82	FOR CLARITY
DRAWN CKL	

TOLERANCE
FINISH
MATERIAL

TITLE: VERSATILE INTERFACE BOARD CIRCUIT DIAGRAM
DRG. No. 100,009C

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